Shashwat Shrivastava

Resume

EPFL
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Interests

I am a Ph.D. student in the Computer and Communication Sciences Department at EPFL. I am broadly interested in FPGA architecture and Computer-Aided Design. My research is focused on reducing the compile time for FPGAs by incorporating architectural enhancements and rethinking CAD algorithms.

Education

2021-Present **Ph.D. in Computer and Communication Sciences**, *EPFL*, Lausanne

2016-2021 **B.Tech. and M.S. by research in Electronics and Communication**, *IIIT-Hyderabad*
Accelerating stereo vision, local Laplacian filters, and CNNs on FPGAs

Work Experience

Sep 2021 - Present **Ph.D.**, *EPFL*
FPGA CAD and Machine Learning

Jun - Dec 2023 **Research Intern**, *AMD*, Longmont, Colorado, USA
Accelerating FPGA routing for commercial architectures

Jan - July 2021 **Research Intern**, *Intel Labs*, Bangalore, India
Hardware-software co-design for 3D image segmentation

May - August 2019 **Student Developer**, *Google Summer of Code Student*, Hyderabad, India
Development of dynamic and interactive robotic simulator

May - July 2018 **Research Intern**, *Bluespec Inc.*, Mysore, India
Hardware design space exploration for dense matrix multiplier

Publications

ICCAD2023 **IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck**
Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar, Dinesh Gaitonde, Mirjana Stojilović

HaSS **Instruction-Level Leakages of Soft-Core CPUs on Shared FPGAs**
Ognjen Glamočanin, **Shashwat Shrivastava**, Jinwei Yao, Nour Ardo, Mathias Payer and Mirjana Stojilović

ACM TACO2022 **An FPGA Overlay for CNN Inference with Fine-grained Flexible Parallelism**
Ziaul Choudhury, **Shashwat Shrivastava**, Lavanya Ramapantulu, Suresh Purini

FPL2021 **FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation**
Shashwat Shrivastava, Ziaul Choudhury, Shashwat Khandelwal, and Suresh Purini

FPL2021 **Accelerating Local Laplacian Filters on FPGAs**
Shashwat Khandelwal, Ziaul Choudhury, **Shashwat Shrivastava**, and Suresh Purini

Teaching Experiences

EPFL

- Fundamentals of Digital Systems, instructor: Dr. Mirjana Stojilović, Spring-2024
- Information, Computation, Communication, instructor: Dr. Mirjana Stojilović, Spring-2022 and Spring-2023
- Computer Architecture, instructor: Dr. Mirjana Stojilović, Fall-2022

IIIT-H

- Intro to Psychology, instructor: Prof. Priyanka Shrivastava, Fall-2020
- Intro to Processor Architecture, instructor: Prof. Suresh Purini, Spring-2020
- Technology Product Entrepreneurship, instructor: Ramesh Loganathan, Fall-2019
- Intro to Internet of Things, instructor: Dr. Lavaya Ramapantulu, Spring-2019
- Embedded Hardware Design, instructor: Dr. Lavanya Ramapantulu, Fall-2018

Honours and Awards

- EPFL EDIC Fellowship
- Dean's List for the year 2017–19, IIIT-H

Technical Skills

Programming Languages: Python, C, C++, Verilog, Bluespec System Verilog, System Verilog, MATLAB, Bash, OpenCL, HLS

Tools: Vivado, Vitis HLS, Xillybus, AWS F1 FPGA, VTR, RunAI

Extracurricular Activities

- Vice President of EPFL PhDs of IC
- Sports coordinator at IIIT-H
- Electronics workshop coordinator at IIIT-H
- Member IIIT-H cricket team

Talks

EPFL 2024 Accelerating ASIC Emulation and Prototyping

ICCAD 2023 IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck

HiPEAC 2023 An FPGA Overlay for CNN Inference with Fine-grained Flexible Parallelism

FPL 2021 FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation